What is claimed is:

1. A circuit comprising:

a first supply node for receiving a first supply voltage and a second supply node for receiving a second supply voltage;

a current mirror connected to the first supply node for providing a first current to a first internal node and a second current to a second internal node;

a first control transistor connected between the first internal node and a second supply node, the first control transistor and the a portion of the current mirror forming a path between the first and second supply nodes, wherein the path includes only two transistors;

a second control transistor and a resistive element connected in series between the second internal node and the second supply node; and

an output unit connected to the current mirror, the output unit including at least one output node for providing at least one reference voltage independent from variations in one of the first and second voltages and independent from variations in a temperature range.

2. The circuit of claim 1, wherein the current mirror includes metal oxide semiconductor transistors.

3. The circuit of claim 2, wherein the first and second control transistors include bipolar transistors.

4. The circuit of claim 3, wherein the first and second control transistors have unequal sizes.

5. The circuit of claim 1 further comprising at least one parasitic transistor connected between the current mirror and one of the first and second control transistors.

6. The circuit of claim 1, wherein the output unit includes:

an output transistor connected to the current mirror; and

an output control transistor and an output resistive element connected in series between the output control transistor and the second supply node.

7. The circuit of claim 6, wherein one of the first, second, and output control transistors is a vertical bipolar transistor having triple-well structure.

8. The circuit of claim 1 further comprising a second output unit connected to the current mirror for providing a second reference voltage.

9. The circuit of claim 1 further comprising:

a transistor connected to the current mirror; and

an output current mirror connected to the transistor for providing a second reference voltage referenced to a voltage at the first supply node.

10. The circuit of claim 1 further comprising a startup unit connected to the current mirror and the first and second control transistors for allowing the at least one reference voltage to switch between a first stable voltage level and a second stable voltage level.

11. The circuit of claim 10, wherein the startup unit includes a capacitor and transistor combination connected to the first internal node for influencing the first and second currents.

12. A circuit comprising:

a first supply node and a second supply node;

a current generating unit connected to the first and second supply nodes for providing a generated current, the current generating unit includes a current path connected between the first and second supply nodes, wherein the current path includes only two transistors; and

an output unit connected to the current generating unit for receiving a version of the generated current for generating at least one bandgap reference voltage.

13. The circuit of claim 12, wherein the current generating unit includes:

a current mirror connected to the first supply node;

a first bipolar transistor connected to the current mirror and the second supply node; and

a second bipolar transistor and a resistive element connected in series between the current mirror and the second supply node.

14. The circuit of claim 13, wherein the first and second bipolar transistors are NPN bipolar transistor.

15. The circuit of claim 14, wherein the first and second bipolar transistors have unequal sizes.

16. The circuit of claim 14, wherein the NPN bipolar transistors are vertical NPN bipolar transistors.

17. The circuit of claim 12 further comprising a second output unit connected to the current generating unit for generating a second bandgap reference voltage.

18. The circuit of claim 17, wherein the second output unit includes an output current mirror.

19. The circuit of claim 12 further comprising a startup unit connected to the current generating unit for allowing the at least one bandgap reference voltage to switch between a first stable voltage level and a second stable voltage level.

20. The circuit of claim 19, wherein the startup unit includes first transistor and a second transistor connected in series with the first transistor between the first and second supply nodes.

21. The circuit of claim 20, wherein the first transistor has a channel length greater than a channel length of the second transistor.

22. A circuit comprising:

a first current source transistor having a source connected to a first supply node, a drain connected to a first internal node, and a gate connected to a second internal node;

a second current source transistor having a source connected to the first supply node, and a drain and a gate connected together at the second internal node;

a first control transistor having a base and a collector connected together at the first internal node, and an emitter connected to a second supply node;

a second control transistor having a base connected to the first internal node, a collector connected to the second internal node, and an emitter;

a first resistive element connected between the emitter of the second control transistor and the second supply node;

an output transistor having a source connected to the first supply node, a gate connected to the second internal node, and a drain connected to an output node;

an output control transistor having a base and a collector connected together, and an emitter connected to the second supply node; and

an output resistive element connected between the collector of the output control transistor and the output node.

23. The circuit of claim 22, wherein first and second source transistors include metal oxide semiconductor transistors

24. The circuit of claim 23, wherein the first, second, and output control transistors are NPN bipolar transistors.

25. The circuit of claim 24, wherein at least one of the NPN bi-polar transistors is a vertical NPN bi-polar transistor having a triple-well structure.

26. The circuit of claim 24, wherein the first control transistor has a first size, and a second control transistor has a second size greater than the first size.

27. The circuit of claim 22 further comprising a second output unit connected to the first and second supply nodes and the second internal nodes for providing a second reference voltage.

28. The circuit of claim 22 further comprising:

a transistor and a current mirror combination connected to the first and second supply nodes and the second internal nodes for providing a second reference voltage referenced to a voltage at the first supply node.

29. The circuit of claim 22 further comprising a startup unit connected to the first and second current source transistors and the first and second control transistors for influencing currents sourced by the first and second source transistors.

30. The circuit of claim 29, wherein the startup unit includes a capacitor and a first transistor combination connected to the first internal node for influencing the currents sourced by the first and second source transistors.

31. The circuit of claim 30, wherein the startup unit includes a second transistor connected to the capacitor and the first transistor.

32. The circuit of claim 31, wherein the startup unit further includes third transistor connected in series with the second transistor between the first and second supply nodes.

33. The circuit of claim 32, wherein the third transistor has a channel length greater than a channel length of the second transistor.

34. A regulator comprising:

a reference circuit for receiving a supply voltage for generating a reference voltage; and

a power unit connected to the reference circuit for generating at least one internal voltage, wherein the reference circuit includes:

a first supply node and a second supply node;

a current generating unit connected to the first and second supply nodes for providing a generated current, the current generating unit includes a current path connected between the first and second supply nodes, wherein the current path includes only two transistors; and

an output unit connected to the current generating unit for receiving a version of the generated current for generating the reference voltage.

35. The regulator of claim 34, wherein the current generating unit includes:

a current mirror connected to the first supply node;

a first bipolar transistor connected to the current mirror and the second supply node; and

a second bipolar transistor and a resistive element connected in series between the current mirror and the second supply node.

36. The regulator of claim 34 further comprising a startup unit connected to the current generating unit for allowing the reference voltage to switch between a first stable voltage level and a second stable voltage level.

37. The regulator of claim 34, wherein the power unit includes at least one amplifying unit for amplifying the reference voltage to generate the at least one internal voltage.

38. A memory device comprising:

a memory array; and

a voltage regulator connected to the memory array for supplying an internal voltage to the memory array, the voltage regulator including a reference circuit for generating a reference voltage to influence the internal voltage, the reference circuit including:

a first supply node and a second supply node;

a current generating unit connected to the first and second supply nodes for providing a generated current, the current generating unit includes a current path connected between the first and second supply nodes, wherein the current path includes only two transistors; and

an output unit connected to the current generating unit for receiving a version of the generated current for generating the reference voltage.

39. The memory device of claim 38, wherein the current generating unit includes:

a current mirror connected to the first supply node;

a first bipolar transistor connected to the current mirror and the second supply node; and

a second bipolar transistor and a resistive element connected in series between the current mirror and the second supply node.

40. The memory device of claim 38 further comprising a startup unit connected to the current generating unit for allowing the reference voltage to switch between a first stable voltage level and a second stable voltage level.

41. The memory device of claim 38, wherein the regulator further includes at least one amplifying unit for amplifying the reference voltage to generate the at least one internal voltage.

42. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including a memory array and a voltage regulator for providing an internal voltage to the memory array, the voltage regulator including a reference circuit, the reference circuit including:

a first supply node and a second supply node;

a current generating unit connected to the first and second supply nodes for providing a generated current, the current generating unit includes a current path connected between the first and second supply nodes, wherein the current path includes only two transistors; and

an output unit connected to the current generating unit for receiving a version of the generated current for generating at least one bandgap reference voltage.

43. The system of claim 42, wherein the current generating unit includes:

a current mirror connected to the first supply node;

a first bipolar transistor connected to the current mirror and the second supply node; and

a second bipolar transistor and a resistive element connected in series between the current mirror and the second supply node.

44. The system of claim 42 further comprising a startup unit connected to the current generating unit for allowing the at least one bandgap reference voltage to switch between a first stable voltage level and a second stable voltage level.

45. The system of claim 42, wherein the regulator further includes at least one amplifying unit for amplifying the at least one bandgap reference voltage to generate the at least one internal voltage.

46. A method comprising:

generating a generated current in a current path of a current generating unit having elements with positive temperature coefficient and elements with negative temperature coefficient, the current path having only two transistors connected in series between a first supply node and a second supply node;

generating at least one reference current based on the generated current; and

generating at least one reference voltage based on the at least one reference current.

47. The method of claim 46, wherein the at least one reference current and the generated current are proportional.

48. The method of claim 46, wherein the reference voltage has a first stable voltage level and a second stable voltage level lower than the first stable voltage

level, and wherein the reference voltage is at the first stable voltage level when one of the supply nodes has a voltage of about 1.3 volts.

49. The method of claim 48, wherein the first stable voltage level is a fixed voltage between about 1.1 volts and about 1.25 volts

50. The method of claim 46 further comprising:

generating a second reference voltage.

51. The method of claim 50 wherein generating a second reference voltage includes generating a second reference current based on the generated current.

52. The method of claim 50 wherein generating a second reference voltage includes:

mirroring the generated current to produce a mirrored current; and

mirroring the mirrorred current to generate the second reference current.

53. The method of claim 46, wherein generating a generated current includes:

influencing the generated current allow the at least one reference voltage to switch from a first stable voltage level to a second stable voltage level; and

stopping the influencing the generated current when the at least one reference voltage reaches the second stable voltage level.

54. A method comprising:

sourcing a first current using a first transistor connected directly to a supply node;

passing the first current directly through a first control transistor connected directly to a second supply node;

sourcing a second current using a second transistor connected directly to the first supply node;

passing the second current directly through a combination of a second control transistor and a resistive element connected to the second supply node;

generating a reference current based on the first and second currents; and

generating a reference voltage based on the reference current.

55. The method of claim 54, wherein the reference current and the first and second currents are proportional.

56. The method of claim 54, wherein the reference voltage has a low stable voltage level and a high stable voltage level higher than the low stable voltage level, and wherein the reference voltage is at the high stable voltage level when one of the supply nodes has a voltage of about 1.3 volts.

57. The method of claim 56, wherein the high stable voltage level is a selected voltage in a range of about 1.1 volts to about 1.25 volts

58. The method of claim 54, wherein generating a reference voltage includes:

influencing the first and second current to allow the reference voltage to switch from a low stable voltage level to a high second stable voltage level; and

stopping the influencing the first and second currents when the reference voltage reaches the high stable voltage level.

59. The method of claim 54 further comprising:

generating a second reference voltage.

60. The method of claim 59, wherein reference voltage is referenced to a voltage at the first supply node.

61. The method of claim 60, wherein second reference voltage is referenced to a voltage at the second supply node.